Amendments to the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of pending United States Patent Application No. 10/231,680, filed August 29, 2002. --

Please replace the paragraph beginning on page 1, line 9 with the following amended paragraph:

As is well known in the art and shown in Figure 1, a DRAM cell 100 typically comprise a capacitor 104 and access transistor 108 pair. One plate of the capacitor 104 is connected to a common cell plate (not shown) to which all capacitors in that DRAM cell array are connected, a subset of which ~~112~~ is shown in Figure 1. The other plate of the capacitor 104 is coupled to a drain of the access transistor 108. The gate of the access transistor 108 is connected to a word line 116 which allows all the DRAM cells coupled to each word line 116 to be activated, while the source of the access transistor 108 is coupled to a digit line 120 which the DRAM cell 100 will read from and write to during memory operations. Activating the gate of the access transistor allows a high voltage charge (Vcc) or low voltage charge (ground) carried by the digit line 120 to pass to the capacitor 104, thus writing the voltage of the digit line 120 to the capacitor 104.

Please replace the paragraph beginning on page 8, line 18 with the following amended paragraph:

Added to this system is a selective cell plate coupling transistor 330 which is coupled to a controller 332. The transistor 330 has one of its terminals coupled through signal line 334 to all of the odd-numbered sub-arrays 302 and the other of its terminals coupled through signal line 336 to all of the even-numbered sub-arrays 302. The controller 332 receives signals generated by other circuitry in a DRAM providing an indication of when a memory read operation is to occur, such as from a row active line 337. For example, as shown in Figure 3A, an active circuit 339 is coupled to the sub-arrays 302 for activation thereof, and is further

coupled to the controller 332 to provide a signal to the controller 332 via the row active line 337 that is indicative of when a memory operation is to occur. The controller 332 normally applies a signal to the gate of the transistor 330 to turn ON the transistor 330. The transistor 330 and signal lines 334, 336 then couple the cell plates 310 of all of the odd-numbered sub-arrays 302 to the cell plates 310 of all of the even-numbered sub-arrays 302. Thus, in this condition, the cell plates of adjacent sub-arrays 302 are coupled to each other. A $V_{CC}/2$ generator 338 is coupled to the signal line 336 to bias the cell plates 310 of the even sub-arrays 302 to $V_{CC}/2$. Of course, when the transistor 330 is ON, the $V_{CC}/2$ generator 338 is also coupled to the signal line 334 to bias the cell plates 310 of the odd sub-arrays 302 to $V_{CC}/2$. The large capacitance of the cell plates 310 allows the voltage of the cell plates 310 for the odd-numbered sub-arrays 302 to remain essentially constant at $V_{CC}/2$.